CS-200 – Computer Architecture
Fall 2025

Week		Date	Time	Room	Lecture	Lab	Deadline
1	Mon	08.09.25	1pm - 3pm	INF1 - INF3		No labs	
	Wed	10.09.25	10am - noon	SG1	Introduction + 1a. Instruction Set Architecture (ISA Reminder, Assembly Language, Compilers)		
	Wed	10.09.25	1pm - 3pm	INF1 - INF3		Introduction to the infrastructure	
	Fri	12.09.25	10am - noon	BCH 2201	1b. Instruction Set Architecture (Branches, Functions, and Stack)		Friday 12.09: Lab A (published)
2	Mon	15.09.25	1pm - 3pm	INF1 - INF3		Lab A (Game of Life)	
	Wed	17.09.25	10am - noon	SG1	1c. Instruction Set Architecture (Memory and Addressing Modes)		
	Wed	17.09.25	1pm - 3pm	INF1 - INF3		Lab A (Game of Life)	
	Fri	19.09.25	10am - noon	BCH 2201	1c. Instruction Set Architecture (Memory and Addressing Modes; cont'd) + 1d. Instruction Set Architecture (Arrays and Data Structures)		
3	Mon	22.09.25			Holiday		
	Wed	24.09.25	10am - noon	SG1	1e. Instruction Set Architecture (Arithmetic)		
	Wed	24.09.25	1pm - 3pm	INF1 - INF3		Exercises on Processors & ISA	
	Fri	26.09.25	10am - noon	BCH 2201	1e. Instruction Set Architecture (Arithmetic; cont'd)		
4	Mon	29.09.25	1pm - 3pm	INF1 - INF3		Lab A (Game of Life)	
	Wed	01.10.25	10am - noon	SG1	2a. Processor, I/Os, and Exceptions (Multicycle Processor)		
	Wed	01.10.25	1pm - 3pm	INF1 - INF3		Lab A (Game of Life)	
	Fri	03.10.25	10am - noon	BCH 2201	2b. Processor, I/Os, and Exceptions (Inputs and Outputs)		
5	Mon	06.10.25	1pm - 3pm	INF1 - INF3		Lab A (Game of Life)	
	Wed	08.10.25	10am - noon	SG1	2c. Processor, I/Os, and Exceptions (Interrupts) + 2d. Processor, I/Os, and Exceptions (Exceptions)		
	Wed	08.10.25	1pm - 3pm	INF1 - INF3		Lab A (Game of Life)	
	Fri	10.10.25	10am - noon	BCH 2201	2d. Processor, I/Os, and Exceptions (Exceptions; cont'd)		Sunday 12.10 @ 23:59: Lab A (final)
6	Mon	13.10.25	1pm - 3pm	INF1 - INF3		Exercises on I/Os and Exceptions	Monday 13.10: Lab B (published)
	Wed	15.10.25	Video		2e. Processor, I/Os, and Exceptions (An Example of I/Os and Exceptions)		
	Wed	15.10.25	1pm - 3pm	INF1 - INF3		Lab B.1 (RISC-V Multicycle Processor): ALU	
	Fri	17.10.25	Video		3a. Memory Hierarchy (Caches)		
7	Mon	27.10.25	1pm - 3pm	INF1 - INF3		Lab B.2 (RISC-V Multicycle Processor): Core	
	Wed	29.10.25	10am - noon	SG1	3a. Memory Hierarchy (Caches; cont'd)		
	Wed	29.10.25	1pm - 3pm	INF1 - INF3		Lab B.2 (RISC-V Multicycle Processor): Core	
	Fri	31.10.25	10am - noon	BCH 2201	3b. Memory Hierarchy (Simple Cache Examples) + 3c. Memory Hierarchy (Virtual Memory)		Sunday 02.11 @ 23:59: Lab B.1 (partial)
8	Mon	03.11.25	1pm - 3pm	INF1 - INF3		Lab B.2 (RISC-V Multicycle Processor): Core	
	Wed	05.11.25	10am - noon	SG1	3c. Memory Hierarchy (Virtual Memory; cont'd) + 3d. Memory Hierarchy (Simple Virtual Memory Examples)		
	Wed	05.11.25	1pm - 3pm	INF1 - INF3		Exercises on Memory Hierarchy	
	Fri	07.11.25	10am - noon	BCH 2201	4a. Instruction-Level Parallelism (Performance) + 4b. Instruction-Level Parallelism (Basic Pipelining)		
9	Mon	10.11.25	1pm - 3pm	INF1 - INF3		Lab B.3 (RISC-V Multicycle Processor): Memory, Peripherals, and Integration	
	Wed	12.11.25	10am - 1:15pm	TBA	Midterm		
	Wed	12.11.25					
	Fri	14.11.25	10am - noon	BCH 2201	4c. Instruction-Level Parallelism (Pipelining)		
10	Mon	17.11.25	1pm - 3pm	INF1 - INF3		Lab B.3 (RISC-V Multicycle Processor): Memory, Peripherals, and Integration	
	Wed	19.11.25	10am - noon	SG1	4c. Instruction-Level Parallelism (Pipelining; cont'd)		
	Wed	19.11.25	1pm - 3pm	INF1 - INF3		Lab B.3 (RISC-V Multicycle Processor): Memory, Peripherals, and Integration	
	Fri	21.11.25	10am - noon	BCH 2201	4d. Instruction-Level Parallelism (Dynamic Scheduling)		Sunday 23.11 @ 23:59: Lab B.2 (partial)
11	Mon	24.11.25	1pm - 3pm	INF1 - INF3		Lab B.3 (RISC-V Multicycle Processor): Memory, Peripherals, and Integration	Monday 24.11: Lab C (published)
	Wed	26.11.25	10am - noon	SG1	4d. Instruction-Level Parallelism (Dynamic Scheduling; cont'd) + 4e. Instruction-Level Parallelism (Examples of Scheduling)		
	Wed	26.11.25	1pm - 3pm	INF1 - INF3		Lab C.1 (RISC-V Interrupts): Adding Interrupt Support	
	Fri	28.11.25	10am - noon	BCH 2201	4e. Instruction-Level Parallelism (Examples of Scheduling; cont'd) + 4f. Instruction-Level Parallelism (Besides and Beyond Superscalars)		Sunday 30.11 @ 23:59: Lab B (final)
12	Mon	01.12.25	1pm - 3pm	INF1 - INF3		Lab C.1 (RISC-V Interrupts): Adding Interrupt Support	
	Wed	03.12.25	10am - noon	SG1	4f. Instruction-Level Parallelism (Besides and Beyond Superscalars; cont'd)		
	Wed	03.12.25	1pm - 3pm	INF1 - INF3		Exercises on Instruction-Level Parallelism	
	Fri	05.12.25	10am - noon	BCH 2201	4f. Instruction-Level Parallelism (Besides and Beyond Superscalars; cont'd) + 4g. Instruction-Level Parallelism (Intel x86 and ARM)		
13	Mon	08.12.25	1pm - 3pm	INF1 - INF3		Lab C.2 (RISC-V Interrupts): Interrupt Controller and Integration	
	Wed	10.12.25	10am - noon	SG1	5a. Multiprocessors (Cache Coherence)		
	Wed	10.12.25	1pm - 3pm	INF1 - INF3		Lab C.2 (RISC-V Interrupts): Interrupt Controller and Integration	
	Fri	12.12.25	10am - noon	BCH 2201	5a. Multiprocessors (Cache Coherence; cont'd) + 5b. Multiprocessors (Examples of Cache Coherence)		Sunday 14.12 @ 23:59: Lab C.1 (partial)
14	Mon	15.12.25	1pm - 3pm	INF1 - INF3		Lab C.2 (RISC-V Interrupts): Interrupt Controller and Integration	
	Wed	17.12.25	10am - noon	SG1	5c. Multiprocessors (Memory Consistency)		
	Wed	17.12.25	1pm - 3pm	INF1 - INF3		Exercises on Multiprocessors	
	Fri	19.12.25	10am - noon	BCH 2201	6. Hardware Security		Sunday 21.12 @ 23:59: Lab C (final)